08-14-00. A1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Commissioner of Patents and Trademarks
Washington, D.C. 20231

PATENT FILING TRANSMITTAL

Transmitted herewith for filing is the Patent Application of: Heinz BAIER

For: METHOD AND SYSTEM FOR PROGRAMMING FPGAs ON PC-CARDS WITHOUT ADDITIONAL HARDWARE

TYPE OF FILING

This new patent application is for a(n):

[X] Utility
[ ] Design
[ ] Plant
[ ] Divisional
[ ] Continuation
[ ] Continuation-in-part

Benefit of a prior filed application

[ ] This application claims the benefit of an earlier filed U.S. Patent Application under 35 USC 120.
[X] Please accord Applicant the benefit of the priority date of 11 August 1999 to this case pursuant to 35 USC 119. Applicant's claim for priority is based on application 99115963.3 filed in the European Patent Office on that date.

Filing under 37 CFR 1.53 (Utility) or 37 CFR 1.153 (Design)

[X] This is an application filed pursuant to 37 CFR 1.53 or 37 CFR 1.153, permitting receipt of a filing date upon filing of a specification, at least one claim and necessary drawings.
[X] In the event any parts of this application are incomplete, please treat this as a filing under 37 CFR 1.53 or 37 CFR 1.153.

ENCLOSURES

[X] 11 - pages of written description;
[X] 3 - pages of claims;
[X] 1 - pages of abstract;
[ ] 2 - sheets of formal drawings;
[X] ___ - sheets of informal drawings;
[X] Declaration and Power of Attorney or listing of inventors;
and
[X] Two postcards for return to us as proof of receipt of the above documents.

plus
[ ] An Assignment of the invention to IBM Corporation and an Assignment cover sheet;

[ ] Verified Statement Claiming Small Entity Status (37 CFR 1.9(f) and 1.27(b))
[X] Form PTO-1449 (IDS) and two copies of the references listed thereon;
[X] A certified copy of EP99115963.3 (country) patent application number (priority document).
[ ] A preliminary amendment;
[ ] Declaration of Biological Deposit;
[ ] Submission of sequence listing, computer readable copy and/or amendment relating thereto for biotechnology invention containing nucleotide and/or amino acid sequence;
[ ] An associate power of attorney;
[ ] Other

DECLARATION OR OATH

The enclosed Declaration or Oath has been executed by:
[ ] Inventor(s);
[ ] Legal representative of the inventors (37 CFR 1.42 or 1.43);
[ ] Joint inventor or person showing proprietary interest on behalf of an inventor who refused to sign or who cannot be reached and this is a petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is attached;
[X] Has not been executed and is enclosed for the purposes of identifying the inventors.

INVENTORSHIP STATEMENT

The inventorship for all the claims in this application is:
[X] the same;
[ ] not the same and, as an explanation, a statement is/ will be submitted.

LANGUAGE

The application submitted herewith is:
[X] in English;
[ ] in not in English and in terms of 37 CFR 1.52(d) a verified translation is
  [ ] attached
  [ ] not attached.

FEE CALCULATION

The filing fee has been calculated as shown below:

				OTHER THAN A	
		SMALL ENTITY	OR	SMALL ENTITY	
BASIC FEE Design Patent		*$155*	$	$310	$
BASIC FEE Utility Patent		$345	$	$690	$690
EXTRA FEES		RATE	FEE	RATE	FEE
TOTAL CLAIMS 4 MINUS 20=	0	x 9=	$0	x18=	$
INDEP.CLAIMS 3 MINUS 3 =	0	x 39=	$0	x78=	$
[ ] MULTIPLE DEP.CLAIM		+135=	$	+270=	$
[ ] ASSIGNMENT		+ 40=	$	+40=	$
[ ] RULE 53 SURCHARGE		+ 65=	$	+130=	$
TOTAL			$		$690

FEE PAYMENT

[X] Attached is Check No. 5644 in the sum of $ 690.00 to cover the filing fee and, if applicable, the assignment fee.

Respectfully submitted,

Dated: August 11, 2000

Stanley D. Ference III
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PATENT

Docket No. DE9-1999-0050US1
(590.018)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	: Heinz BAIER	Group Art: not yet assigned
Serial No.	: not yet assigned	Examiner: not yet assigned
Filed	: herewith	
For	: METHOD AND SYSTEM FOR PROGRAMMING FPGAs ON PC-CARDS WITHOUT ADDITIONAL HARDWARE	

EXPRESS MAIL CERTIFICATE

Express Mail Label No. EL503717346US

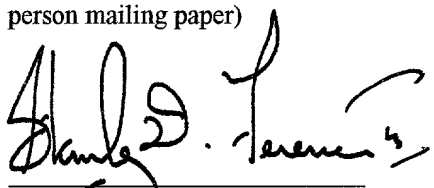
Date of Deposit 11 August 2000

I hereby certify that the following attached paper(s) or fee:

Patent Application
Written Description
Claims 1-4
Abstract
Drawings (Figs. 1-3)
Declaration and Power of Attorney (unexecuted)
Information Disclosure Statement
PTO Form 1449, with two copies of cited references
Certified Copy of Priority Document
Patent Filing Transmittal
Certificate of Express Mail
Check in the Amount of $690 (Check No. 5644)
Two Return Postcards

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Stanley D. Ference III
(Typed or printed name of person mailing paper)



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METHOD AND SYSTEM FOR PROGRAMMING FPGAs ON PC-CARDS WITHOUT ADDITIONAL HARDWARE

Claim for Priority

This application claims priority from European Application No. 99115963.3, filed on August 11, 1999, which is hereby incorporated by reference.

Field of the Invention

The present invention relates to the area of programming field programmable gate arrays. In particular, the present invention relates to improve the usage of same during the use by end-users and during development of circuits implementing some new functionality on said field programmable arrays.

Background of the Invention

In general, field programmable arrays, further referred to herein and abbreviated as FPGA, are used to implement some computing functionality which is intended to run basic, hardware related functions used to control the basic functions of computer periphery, which recognizes video screens, printers, network cards, etc.

Further, FPGAs are used in applications which require a vast amount of basic arithmetic computations, e.g., multiplication and addition operations, that have to be performed very quickly in graphic processing applications.

FPGAs are used to implement computational functionality which is implemented in a large number (up to 1 million) of inter-connected circuits. Such vast cicuits are planned and realized with the help of a special hardware, e.g., the hardware device of Byte BlasterMV, which is connected to either the serial or the parallel port of the workstation used in turn as a development platform with dedicated software tools.

This is depicted in Figure 2, where a PCI card is shown schematically connected to extra hardware 32 external to the PC. Logic 34 is provided for controlling and programming the FPGA 16 with the configuration data to be developed for the FPGA and feeding it with the configuration data necessary for the PCI card to be detected by the bus system on a system start-up. Such prior art development environments require either additional hardware or Programmable Read Only Memory devices, further referred to herein as PROMs. The developed schema containing the new functionality is fed into the PROM which is placed onto the PC-card to be developed comprising the FPGA. After a subsequent POWER-On of the developer's workstation, the PROM controls and performs the configuration of the FPGA. Then, the functionality of the FPGA can be tested during

operation. If a further update of the schema is necessary, a new PROM has to be used, as the used one can not be rewritten.

Alternatively, Electrical Erasable PROMs, further referred to herein as EEPROMS are used instead of PROMs. They can be rewritten in case of a further update, however, external hardware is necessary in order to control the write process into the EEPROM.

During development of FPGA functionality, or when an end-user exchanges a PC-card comprising said FPGA due to any update or extension of functionality incorporated in his card, manual access to the concerned card is necessary. In the case of a FPGA developer, manual access is needed to replace at least the PROM used to program the FPGA. In the latter instance, manual access to the concerned card is necessary in order to replace the card by another. The same basically applies when instead of an update, any new functionality is implemented on an FPGA.

Any manual access to PC-cards, however, causes additional work and bears the risk to damage other hardware connected in the casing of the computer, e.g., by statical charges brought to any of a plurality of locations sensitive thereto.

Summary of the Invention

The present invention broadly contemplates a method and circuit in order to improve the usage of FPGAs during the use by end-users and during development of circuits implementing some new functionality on said FPGAs. In accordance with the present invention, programming and updating hardware electronic circuits is accomplished without manually accessing the circuits.

In accordance with one aspect of the invention, a PROM or a EEPROM device is physically connected onto the concerned card. This device is intended to be accessed serially and to input a serial data stream into the FPGA, which is necessary when the FPGA shall be notified to the bus system of the computer, e.g., a PCI bus, and in order to be able to access a card via a conventional device driver. As mentioned above, the FPGA is automatically configured by the PROM on the next Power-On of the computer which represents a requirement for the PCI-card to be detected properly by the BIOS of the computer.

In another aspect of the present invention, there exists a hardware circuit arrangement comprising an EEPROM device, and a FPGA device which is accessible via a computer bus system and a multiplexer which allows several users to share communication

channels such as outgoing phone lines, hereinafter referred to as a MUX element connected between said devices.

Another aspect of the present invention includes a circuit arrangement of the PROM device arranged for comprising control data for proper recognition of the FPGA by said bus system, and which recognizes a compromise to a logic usable to recognize programming a EEPROM device with an EEPROM-FPGA interface like that of Joint Test Action Group (JTAG). In accordance with the present invention, the above mentioned MUX element can be controlled to select either said PROM device or said EEPROM device or said FPGA device for reading data from said devices, in order to properly connect said FPGA to said bus system and to initialize a configuration of said FPGA with the contents comprised of said EEPROM.

In another aspect of the present invention, a method is provided to perform various updates of the FPGA contents without accessing the card physically. In accordance with this method, during a first sequence of steps the FPGA is used to program the EEPROM with the schema received from a disk. Then, the MUX is switched to be able to read from the EEPROM and feed the developed schema programmed therein into the FPGA as it was intended originally. The PROM is just used to deliver the information to the FPGA which is necessary for the PC-card to be recognized by the BIOS on a first start-up. Thus,

a characteristic feature of the present invention is that the FPGA device is configured in a double way, first in order to initialize the desired disk communication and then to be re-configured according to the EEPROM contents.

The method and circuit according to the present invention have the advantage, in relation to the method sketched in the discussion of prior art technique in that they allow programming of FPGAs without accessing physically the card comprising the FPGA. Consequently, the average development time is lowered and costs are reduced. A further advantage is that no extra hardware is required external to the computer. Yet, a further advantage is the ability to construct a generic PC-card that can easily be re-programmed in order to perform an extended functionality compared to that before. Or, it is possible to implement a totally different functionality - if desired. Thus, the present invention increases flexibility of FPGA hardware as it is no more dedicated for a sole purpose only.

For a better understanding of the present invention, together with other and further features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, and the scope of the invention will be pointed out in the appended claims.

Brief Description of the Drawings

Fig. 1 is a schematic representation of a structural diagram showing the essential elements of the circuit according a preferred embodiment of the present invention.

Fig. 2 is a schematic representation of a structural diagram showing the essential elements of a circuit according to prior art.

Fig. 3 is a schematic representation of a block diagram showing the essential steps of the method according to a first and a second aspect of the present invention.

Description of the Preferred Embodiment

With general reference to the figures and with special reference now to Fig. 1 the essential elements of the circuit according to the invention are described.

A PROM 10 and an EEPROM 12 are connected via a multiplexer element 14 with an FPGA 16 located on the generic PC-card 18 to be generated according to the present invention. The PC-card 18 is depicted schematically with broken lines. A number of 40 lines are provided at the right side of the FPGA as input/output lines in order to represent the connection to the PCI bus system of the computer.

From both, PROM 10 and EEPROM 12 a clock line 27a CLK and a data line 29a DATA are connected to respective entries of the MUX 14. A clock line 27c and data line 27 are output from the MUX to respective entries in the FPGA 16.

The MUX element 14 can be controlled via a line MUX CTL in order to read data from PROM 10, i.e., when said line is inactive, or from EEPROM 12, when said line is switched active.

Further, there are provided four connections TCK, TDI, TMS and TDO between FPGA 16 and EEPROM 12 in order to program the EEPROM 12 from FPGA 16 as discussed with reference to the prior art cited above.

Further, there is provided a signal line INIT_CONFIG from an output of the FPGA 16 to an input of EPROM 12, the operation of which will be discussed below.

PROM 10 comprises all configuration data necessary to configure the FGPA 16 in order to be recognized by the BIOS as a PCI-bus participating device on a start-up of the computer and to be accessed via a device driver 120. Further, it comprises all logic necessary to program the EEPROM 12 with the JTAG interface as discussed above.

Referring now to Fig. 3, the essential steps of programming the EEPROM 12 and the FPGA 16 are shown.

After Power-On, step 110, the FPGA 16 is configured automatically via the PROM 10 contents, step 120. The FPGA 16 signals its presence after being prompted by the BIOS. The FPGA 16 contains the PCI target device function and can thus communicate with a device driver.

In accordance with a first embodiment of the method of the present invention, the EEPROM 12 used to program the FPGA 16 shall be programmed with a new update of FPGA 16 development schema mentioned above, which corresponds to the YES-branch in decision 130. Any prior art device driver reads the schema, which recognizes the configuration data from a disk 140 to where it was written by the schema development tool and programs these data into the EEPROM 12 via the dedicated function implemented in the FPGA 16 which was mentioned above as program config-data via FPGA 16-implemented function 150.

In particular, like in prior art, the dedicated JTAG signals Clock (TCK), Data Input (TDI), Mode selection (TMS) and Data Output (TDO) as depicted in Fig. 1. Thus, the EEPROM 12 programming is completed.

Then, the configuration process for the FPGA 16 with the contents of the EEPROM 12 is triggered by activating the so-called Card_INIT function via the signal line INIT_CONFIG. Said triggering step is controlled by a function implemented in FPGA 16.

In particular, the MUX 14 is switched in step 160 via the line MUX CTL so that the lines CLK and DATA of the EEPROM 12 are fed into the FPGA 16. When the line INIT_CONFIG is actually activated, step 170, the FPGA 16 will be configured with the contents of the EEPROM 12, step 180. Thus, the FPGA 16 programming is completed with step 190. It can be repeated with a new updated version of the schema by simply repeating the steps just described above.

In accordance with a second embodiment of the method of the present invention, the EEPROM 12 is already re-programmed. Thus, such cases are covered in which the development of a new FPGA 16 configuration schema is completed. In this case the method as depicted in Fig. 3 continues after the start-up procedure, step 110 with PROM 10 involved, step 120, leaves the decision 130 via the NO-branch and continues with step 160 as described above.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are accordingly to be regarded as illustrative rather than in a restrictive sense.

It should be noted that the present invention is independent from the bus system in use with the PC hosting the FPGA schema development environment.

Claims

What is claimed is:

1. A method for programming field programmable gate arrays (FPGA) with configuration data according to a schema developed by a developing a tool on a computer device, the method comprising by the steps of:

(a) reading said schema by a device driver from a storage device of said computer device;

(b) programming said schema by aid of a dedicated function implemented in said FPGA into an electrical erasable programmable read only memory (EEPROM) connected with said FPGA via a multiplexer, hereinafter referred to as a MUX element;

(c) switching said MUX element in order to be able to read from said EEPROM into said FPGA and

(d) triggering the configuration of said FPGA by feeding said schema from said EEPROM to said FPGA.

2. A method for using field programmable gate arrays (FPGAs) with configuration data stored in an electrical erasable programmable read only memory (EEPROM)

connected to said FPGA via a multiplexer, hereinafter referred to as a MUX element, the method comprising the steps of:

(a) controlling said MUX element in order to be able to read from said EEPROM into said FPGA; and

(b) triggering the configuration of said FPGA by feeding said schema from said EEPROM to said FPGA.

3. A hardware circuit arrangement having a programmable read only memory (PROM) device, an electrical erasable programmable read only memory (EEPROM) device, a field programmable grate array (FPGA) device accessible via a computer bus system and a multiplexer, hereinafter referred to as a MUX element, connected between said devices, said circuit arrangement comprising:

(a) said PROM device being arranged for comprising control data for proper recognition of said FPGA by said bus system, and a logic usable for programming said EEPROM device with an EEPROM-FPGA interface;

(b) said MUX element being controllable to select either said PROM device or said EEPROM device or said FPGA device for reading data from said devices, in order to

properly connect said FPGA to said bus system and to initialize a configuration of said FPGA with contents comprised of said EEPROM.

4. The circuit arrangement according to claim 3, wherein a PC-card is detectable by a PC system bus.

METHOD AND SYSTEM FOR PROGRAMMING FPGAs ON PC-CARDS WITHOUT ADDITIONAL HARDWARE

Abstract

Method and circuit arrangements are provided for programming or updating hardware electronic circuits without manually accessing the circuits. The circuit arrangement includes an EEPROM device, a FPGA device which is accessible via a computer bus system and a MUX element connected between said devices. In the circuit arrangement, a PROM device is arranged for comprising control data for proper recognition of the FPGA by the bus system, and for comprising a logic usable for programming the EEPROM device with an EEPROM-FPGA interface like that of Joint Test Action Group (JTAG). The MUX element can be controlled to read data from either the PROM device, EEPROM device, or FPGA device, in order to properly connect the FPGA to the bus for reading date from the bus system and to initialize a configuration of the FPGA with the contents of the EEPROM. In the method of the present invention, the FPGA is used to program the EEPROM with the schema received from a disk. The MUX is switched to be able to read from the EEPROM and feed the developed schema therein into the FPGA. The PROM is used to deliver the information to the FPGA, which is necessary for the PC-card to be recognized by the BIOS on a first start-up.

[drawings)

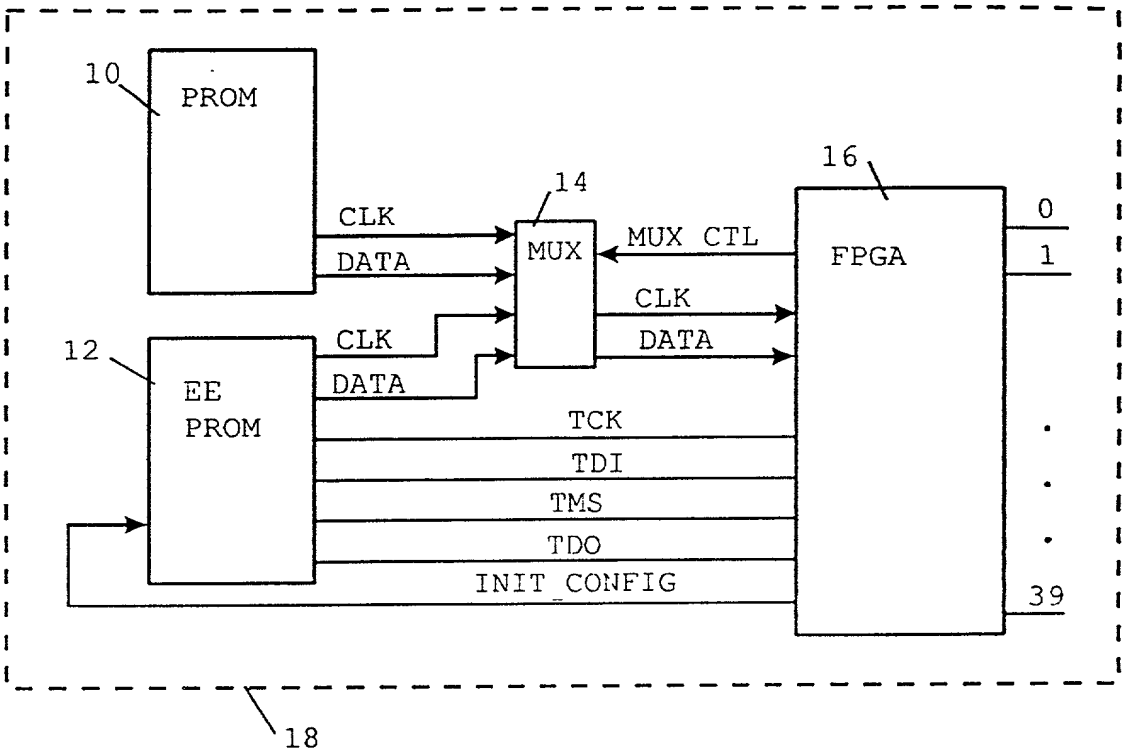

FIG. 1

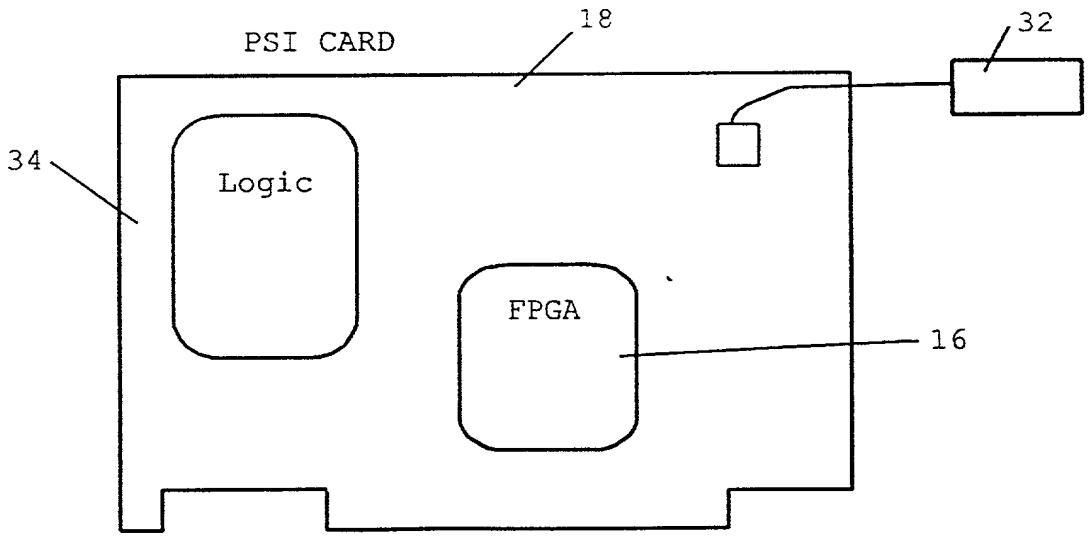

FIG. 2

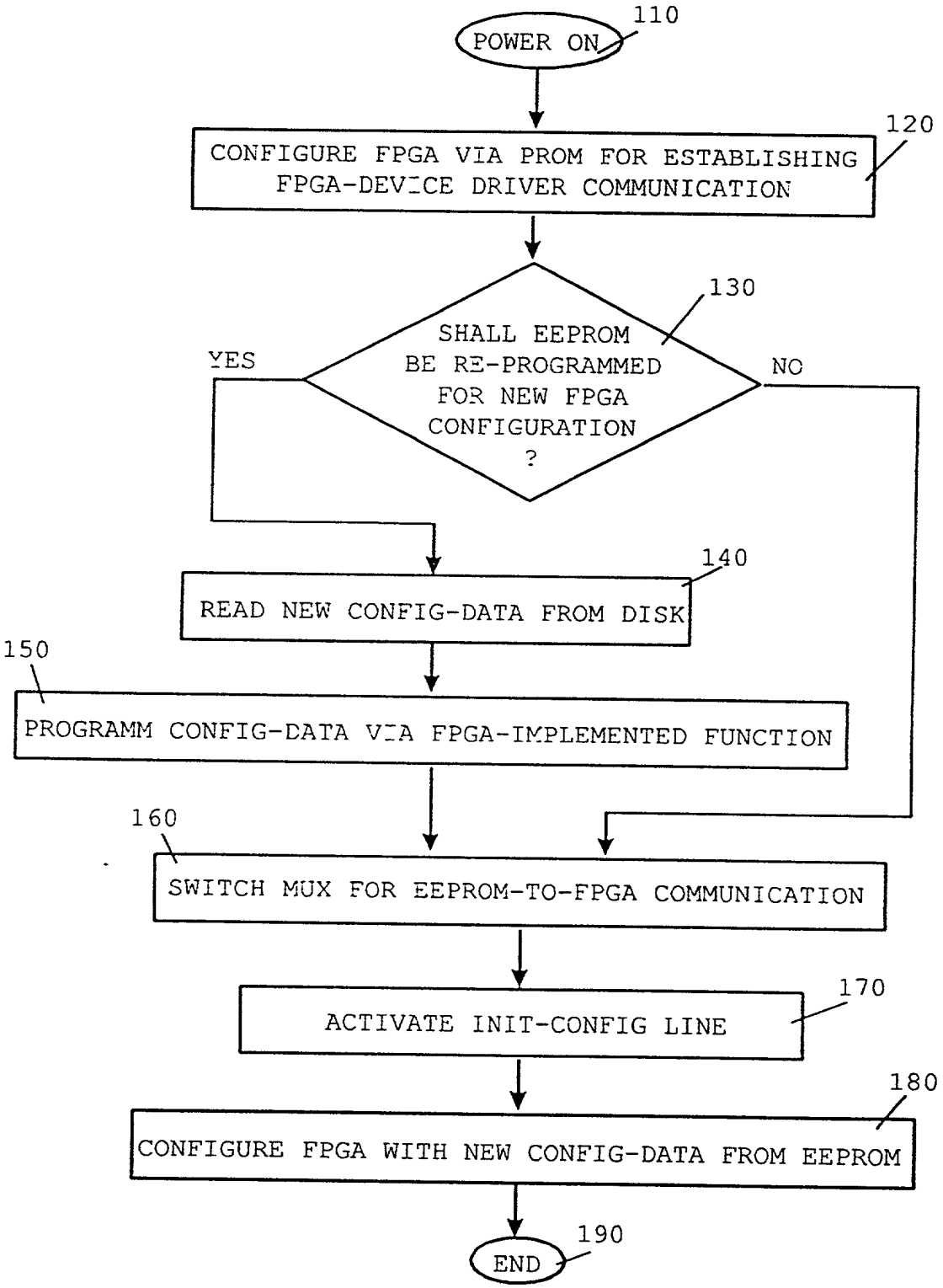
110
POWER ON
120
CONFIGURE FPGA VIA PROM FOR ESTABLISHING FPGA-DEVICE DRIVER COMMUNICATION
130
SHALL EEPROM BE RE-PROGRAMMED FOR NEW FPGA CONFIGURATION ?
YES
NO
140
READ NEW CONFIG-DATA FROM DISK
150
PROGRAMM CONFIG-DATA VIA FPGA-IMPLEMENTED FUNCTION
160
SWITCH MUX FOR EEPROM-TO-FPGA COMMUNICATION
170
ACTIVATE INIT-CONFIG LINE
180
CONFIGURE FPGA WITH NEW CONFIG-DATA FROM EEPROM
190
END

FIG. 3

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND SYSTEM FOR PROGRAMMING FPGAs ON PC-CARDS WITHOUT ADDITIONAL HARDWARE

the specification of which (check one)

____ is attached hereto.

__X__ was filed on 11 August 2000 as International Business Machines Docket No. DE9-1999-0050US1

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application, having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)				Priority Claimed
99115963.3 (Number)	EP (Country)	11/August/1999 (Day/Month/Year Filed)		X Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)		___ Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)		___ Yes ___ No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

DELARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

I hereby claim the benefit under 35 U.S.C. §120 of any United States Application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States, or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

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Direct Telephone Calls to: (name and telephone number) Stanley D. Ference III, (412) 781-7386

Heinz Baier
Full name of sole or first inventor

Inventor's Signature Date

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Citizenship

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